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Amendments to the Claims

1(Currently amended). An apparatus having an integrated circuit, the integrated circuit comprising;

a first circuit having a power supply potential and adapted to store a volatile logic value; and

a second circuit adapted to generate a logic value when coupled to receive a the power supply potential from the first circuit in a first operational mode and decoupled from receiving the power supply potential when the first circuit is not in the first operational mode.

2(Original). The apparatus of claim 1, wherein the integrated circuit further comprises a coupling transistor to couple and decouple the second circuit from the power supply potential.

3(Previously presented). The apparatus of claim 2, wherein the coupling transistor is in series between the second circuit and a node to be coupled to the power supply potential.

4(Original). The apparatus of claim 2, wherein the second circuit comprises a logic transistor having a gate dielectric layer that is thinner than a gate dielectric layer of the coupling transistor.

5(Original). The apparatus of claim 4, wherein the gate dielectric layer of the logic transistor is at least 30 angstroms thinner than the gate dielectric layer of the coupling transistor.

6(Original). The apparatus of claim 2, wherein the integrated circuit further comprises a pass transistor connected in parallel with the coupling transistor, the pass transistor being of the opposite polarity as the coupling transistor.

7(Original). The apparatus of claim 1, wherein the integrated circuit further comprises a voltage regulator and the integrated circuit is adapted to couple the first circuit to the voltage regulator in the first operational mode.

8(Previously presented). The apparatus of claim 7, wherein the integrated circuit is adapted to decouple the power supply potential from the first circuit when in a second operational mode.

9(Original). The apparatus of claim 1, wherein the second circuit is adapted to generate the logic value based at least in part on the volatile logic value.

10(Original). The apparatus of claim 1, wherein the integrated circuit is further adapted to couple the first circuit and the second circuit to the power supply potential in a second operational mode.

11(Original). The apparatus of claim 10, wherein the integrated circuit is further adapted to couple the first circuit and the second circuit to each other in the second operational mode.

12(Previously presented). A method comprising:

supplying a power supply voltage potential to a memory circuit;

coupling the power supply voltage potential from the memory circuit to a logic circuit when an integrated circuit is in a first operational mode; and

retaining a volatile logic value in the memory circuit while decoupling the power supply voltage potential from the logic circuit when the integrated circuit is in a second operational mode.

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13(Withdrawn). The method of claim 12, further comprising coupling the logic circuit and the memory circuit to the power supply voltage potential when the integrated circuit is in a second operational mode.

14(Withdrawn). The method of claim 13, further comprising coupling the logic circuit to the memory circuit.

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~~15~~(Previously presented). The method of claim 12, further comprising coupling the memory circuit to a voltage regulator when the integrated circuit is in the second operational mode.

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~~16~~(Previously presented). The method of claim 12, further comprising generating a logic value with the logic circuit based, at least in part, on a volatile logic value stored in the memory circuit when the integrated circuit is in the first operational mode.

13 17(Previously presented). A computing system comprising:

a static random access memory; and

an instruction processing unit, the instruction processing unit comprising:

a first circuit to receive a power supply potential and store a volatile logic value; and

a second circuit coupled to the first circuit to receive the power supply potential in a first operational mode and generate a logic value, wherein the instruction processing unit decouples the power supply potential from at least a portion of the second circuit in a second operational mode and the first circuit retains the volatile logic value.

16 18(Original). The computing system of claim 15 17, wherein the instruction processing unit further comprises a coupling transistor to couple and decouple the second circuit from the power supply potential.

19(Withdrawn). The computing system of claim 18, wherein the second circuit comprises a coupling transistor having a gate dielectric layer that is at least twice as thick as a gate dielectric layer of the coupling transistor.

17 20(Original). The computing system of claim 15 17, further comprises a voltage regulator, wherein the instruction processing unit is adapted to couple the first circuit to the voltage regulator in the first operational mode.

18 21(Previously presented). The computing system of claim 17 20, wherein the instruction processing unit is adapted to decouple the power supply potential from the first circuit when in the second operational mode.

22(Withdrawn). The computing system of claim 17, wherein the instruction processing unit is further adapted to couple the first circuit and the second circuit to the power supply potential in a second operational mode.

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23(Withdrawn). The computing system of claim 22, wherein the instruction processing unit is further adapted to couple the first circuit and the second circuit to each other in the second operational mode.